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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/239,907
Filing Date: January 29, 1999
Appellant(s): MACCORMACK ET AL.

Mr. Timothy L. Boller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07 June 2007 appealing from the Office action mailed 08 February 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. The after final amendments were not entered as outlined in the Advisory Action mailed 26 April 2006.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,959,659	DOKIC	9-1999
5,844,595	BLATTER et al.	12-1998
5,602,920	BESTLER et al.	2-1997

ADSP-2100 Family User's Manual 3rd Edition (9/95) - Chapter 4: Data Transfer

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1 and 3-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As set forth in the specification as well as applicant's previous arguments, the "third control circuit" corresponds to the illustrated search engine [322] and the input module corresponds to the illustrated input module [100]. The specification sets forth that the search engine generates a match signal responsive to finding a match and subsequently instructs the "second control circuit" or transport processor [320] to access a particular address for information needed so as to control the input module [100] to process the

received signal which may include the particular descrambling of the received information (IA: Page 9, Para 7 – Page 12, Para. 2; Page, 20, Para. 3 – Page 21, Para. 2). The claim sets forth that the "second control circuit" or transport processor [320] further "controls processing of the input data packet responsive to the match signal by the input module". However, as disclosed in the prior section of the specification, while the "second control circuit" is operable to control processing of the input data packet by the input module responsive to the match signal, the match signal is not generated by the input module. Rather, the particular match signal as disclosed in the specification and required by the claim to be generated by the "third control circuit" (ex. a "third control circuit . . . for setting a match signal to the second control circuit responsive to a match"). No further art rejection is being applied in light of the logical inconsistency required by the claim; given that the claim initially sets forth that the "third control circuit" is responsible for generating the match signal and latter claims that the distinctive input module is responsible for the match signal.

2. Claims 39-41, 45, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Dokic (US Pat No. 5,959,659).

Claim 39 is rejected wherein the Dokic reference discloses a "receiver" [100] for "processing a packetized digital data stream". As illustrated in Figures 3 and 5, the "receiver" [100] comprises an "input module" [104] to "receive and process a data packet" associated with an MPEG-2 transport stream" a "memory" [205], and a "receiver processor" [106] to "control storage of desired packet identifiers and associated control information in the memory" (Col 8, Lines 24-31; Col 13, Lines 13-26). The receiver

further comprises a "transport controller" [102] having a "transport processor" [204] to "extract a packet identifier from a packet in the input module" and a "search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory". Subsequently, "responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in memory" such as control information serving to designate the particular packet type and "controls processing of the received data packet by the input module based on the retrieved control information" such that it is directed to the appropriate packet buffer [206/208/210] (Col 7, Line 49 – Col 9, Line 6).

Claim 40 is rejected wherein the "transport processor generates a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory" (Col 8, Lines 53-67).

Claim 41 is rejected wherein the "input module discards a packet in response to the control signal" (Col 8, Lines 64-67).

In consideration of claim 45, Figure 3 of the Dokic reference discloses a "receiver" [100] for "processing a packetized digital data stream". The "means for receiving a data packet" [112/114], a "means for retrieving control information associated with a received data packet" [102], and a "means for controlling processing of a received data packet by the means for receiving a data packet" [106].

Claim 46 is rejected wherein the "means for receiving control information" [102] (Figure 5) comprises a "memory for storing packet identifiers and control information associated with desired packets in the digital data stream" [205] (ex. information

identifying the particular PID as well as information identifying the particular type of PID), a "search engine" and a "transport processor" [204] (Col 8, Lines 7-67).

3. Claims 11 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer.

In consideration of claims 11 and 20, the Dokic reference discloses a method of "demultiplexing" or "decoding a digital data stream" wherein the "digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). The method comprises "inputting the digital data stream" (Figure 3; Col 5, Line 60 – Col 6, Line 9) and "storing in a memory separate from the data stream" [205] (Figure 3) and "under control of a first control circuit" [106], the "packet identifiers that correspond to data packets required by the receiver" (Col 8, Lines 28-31 and 58-60; Col 9, Lines 10-23). The system "extracts under the control of a second control circuit" [204], a "packet identifier from a data packet in the input digital stream", "determines, under the control of a third control circuit" [204] "whether the extracted packet identifier matches one of the stored packet identifiers, sets a match signal responsive to a match determined by the third control circuit", and "demultiplexes under the control of the second control circuit, the input data packet responsive to the match signal" (Col 8, Lines 20-52; Col 9, Lines 18-43).

With respect to the limitation pertaining to "outputting an address", the Dokic reference does not explicitly disclose nor preclude details pertaining to the retrieval of information through a "memory address". The reference explicitly discloses that the

preferred embodiment of the digital signal processor is a DSP2111 manufactured by Analog Devices® (Col 7, Lines 53-55). The ADSP-2100 Family User's Manual – Chapter 4 describes that the circular buffers rely on "addresses" in order to determine where to locate the next piece of information in a circular buffer may be located (Sections 4.2.3 – 4.3.2). Accordingly, it would have obvious to one of ordinary skill at the time of the invention to utilize the teachings of the ADSP-2100 User's Manual such that the embodiment would implicitly "output an address in the memory responsive to a match" in order to know where in the on-board memory [200/202/205] to retrieve the "entire packet" comprising both the identifier and "control information associated with the packet identifier" for the purposes of implementing the preferred embodiment using components explicitly disclosed by Dokic.

As to the limitation pertaining to the "control information", the claimed language is not limiting other than to require that the "control information" is something that is "associated with the packet identifier". The Dokic reference teaches that the MPEG-2 transport stream may comprise packets of "control information" such as the program map table (PMT) or program association table (PAT) from the MPEG-2 transport stream (Col 4, Lines 22-27). These program specific information (PSI) tables are associated with reserved packet identifiers (PID) (ISO/IEC 13818-1: Section 2.4.4). As such, the Dokic reference teaches that the PID from the received packet is parsed from the transport packet to identify the type of data carried by the transport packet. Accordingly, "control information" may be temporarily stored in the packet buffers [200/202] prior to being transferred to the host processor [106] (Col 9, Lines 29-43).

Alternatively, it is further noted that the packet header may further comprise "control information" in the form of timing information (PCR) used in the decoding of the payload. The packet buffers [200/202] or "memory" are disclosed to store the entire transport packet comprising "control information associated with the packet identifier" (Col 7, Lines 66-67 – Col 8, Lines 1-4). The Dokic reference goes on to suggest that either the "entire packet" or the payload may be forwarded from the "memory" (Col 9, Lines 39-43). The claim language is subsequently not limiting such that the "entire packet" comprising both the identifier and the "control information associated with the identifier" contained within the packet header may be "accessed" and "demultiplexed".

Claims 13 and 14 are rejected in view of Figure 5 wherein "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Col 8, Lines 31-37, 53-67). It is taught that should the "input data packets" contain private data, the entire packet will either be "transferred". Alternatively, the packet may be "processed" such that only the payload data is "transferred" (Col 9, Lines 39-53).

Claim 15 is rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 16 and 17 is rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets.

In consideration of claim 18, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Col 2, Lines 29-44; Col 8, Lines 20-31, 48-52).

Claim 19 is rejected wherein the "third control circuit" [204] "systematically" searches the transport packet buffers [200/202] for a "match". Figures 6A-C further illustrate a "systematic" method for "searching the memory" in conjunction with the demultiplexing process.

4. Claims 21-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of Blatter et al. (US Pat No. 5,844,595).

In consideration of claims 21 and 29, as aforementioned, the Dokic reference discloses a decoder that may function as a "set top box" or "receiver for the demultiplexing digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). Figure 3 illustrates a block diagram of the "receiver" architecture comprising: "input circuitry for receiving the digital data stream" [112] (Col 6, Lines 10-12), a demultiplexing section [104], and a control section [108] (Col 5, Line 60 – Col 6, Line 9). The demultiplexing section, as illustrated in Figure 5 comprises a data structure [205] for storing packet identifiers that correspond to data packets required by the receiver (Col 8,

Lines 26-31) and a "first" and "second control circuits" [204] of the digital signal processor [102] for "extracting a packet identifier from a data packet in the digital data stream input", "determining whether such matches one of the packet identifiers in the first data structure", and "responsive to a match" is operable to "demultiplex the input data packet" (Col 8, Lines 20-52; Col 9, Lines 18-43).

The reference, however, does not explicitly disclose nor preclude the particulars pertaining to the "first" and "second data structure" as particularly claimed nor does it disclose the particular usage of encryption/decryption in conjunction with the MPEG-2 transport as is understood in the art. The Blatter et al. reference discloses the usage of encryption/decryption in conjunction with a MPEG demultiplexor comprising a "first" [45] and "second data structure" [45] wherein the "control information" or decryption information associated with the "second data structure" [45] is memory mapped or "accessed based on addressing information extracted from the first data structure" (Col 4, Line 56 – Col 5, Line 19). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the data structure [205] of Dokic reference to comprise a "first" and "second data structure" such as those employed by Blatter et al. such that "responsive to a match" the "addressing information" associated with the "control information" is "outputted" and "retrieved" for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to further provide a low-overhead mechanism by which processes can synchronize and communicate while reducing I/O data movement.

Claims 30 and 38 are rejected in view of the rejection of claims 21 and 29. The "method of demultiplexing a digital data stream" in conjunction with a "set-top-box" is met wherein the reference teaches the following steps: "inputting the digital data stream" (Dokic: Figure 3; Col 5, Line 60 – Col 6, Line 9), "storing . . . packet identifiers required by the receiver in a second data structure" [205] (Col 8, Lines 28-31 and 58-60; Col 9, Lines 10-23), and "determining", "extracting", and "demultiplexing" under the control of a "second" and "third control circuit" packets responsive to a "match" (Dokic: Col 8, Lines 20-52; Col 9, Lines 18-43). As aforementioned, the Dokic reference does not explicitly disclose the particular usage of "outputting addressing information" in conjunction with a "first" and "second data structure". The Blatter et al. reference discloses the usage of a "first" [45] and a "second" data structure" [45] whereupon addressing information from the "second data structure" [45] may be utilized to access "control information" associated with the decryption of packets from the "first data structure" [45]. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dokic reference to further employ a "first" and "second data structure" that employs memory mapping techniques such as those employed by Blatter et al. for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to further provide a low-overhead mechanism by which processes can synchronize and communicate while reducing I/O data movement.

In consideration of claims 22-23 and 31-32, the Blatter et al. reference further discloses that the "control information" further identifies "destination address

information" (Col 5, Lines 5-8). Accordingly, "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Dokic: Col 8, Lines 31-37, 53-67).

Claims 24 and 33 are rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 25-26 and 34-35 are rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets. The instant application further supports this definition (Page 2, Lines 5-8).

In consideration of claims 27 and 36, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Dokic: Col 2, Lines 29-44; Col 8, Lines 20-31 and 48-52).

Claims 28 and 37 are rejected wherein the "first" and "second control circuits" [204] are embedded within a digital signal processor [106] that is coupled to a PAL [118].

Accordingly, the digital signal processor [106] functions as both a "search engine" to identify buffered packets and a "transport processor" to move the packets into the appropriate buffer as aforementioned (Dokic: Col 8, Lines 20-52).

5. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of Bestler et al. (US Pat No. 5,602,920).

In consideration of claim 42, the Dokic reference does not particularly disclose that the "input module" [104] further "descrambles a packet in response to the control signal". The Bestler et al. reference discloses a combined DCAM and transport demultiplexer [20] or "input module" wherein the "input module descrambles a packet in response to the control signal" (Bestler et al.: Col 3, Lines 7-44; Col 4, Lines 25-59; Col 4, Line 66 – Col 5, Line 17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made so as to modify the "input module" [104] so as to further comprise a descrambler which "descrambles a packet in response to the control signal" for the purpose of providing/enabling greater flexibility in the types of programming (ex. premium, PPV, or other forms of scrambled programming) with which the Dokic system can process and to particularly do so using a single circuit optimized to perform both demultiplexing and conditional access functions (Bestler et al.: Col 1, Lines 49-67).

(10) Response to Argument

The examiner respectfully disagrees that the rejection should be reversed. The Examiner's Answer only addresses arguments for patentability made appellant. Any further

arguments regarding other elements or limitations not specifically argued that the appellant could have made are not being addressed further for consideration by the panel. Should the panel find that the examiner's position/arguments or any aspect of the rejection is not sufficiently clear or a particular issue is of need of further explanation, it is respectfully requested that the case be remanded to the examiner for further explanation prior to the rendering of a decision.[1]

A. Rejection of claims 1 and 3-10 under 35 U.S.C. 112 1st paragraph

Appellant argues that the examiner erred based on a misinterpretation of the claims in that claims 1 and 10 do not recite an input module setting a match signal. Rather, appellant's argue that the 'third control circuit' sets the match. The examiner does not disagree that the claim initially recites that the 'third control circuit' sets the match. However, claim 1 explicitly later recites that "the second control circuit . . . controls processing of the input data packet responsive to the match signal by the input module". Claim 10 similarly states that the "the second control circuit . . . controls processing of the input data packet responsive to the match signal by the input module". As noted in the rejection, this creates a logical inconsistency because the same match signal is generated by both the third control circuit and the input module. This not described / enabled in the specification as originally filled and appellants do not appear to contest that that support for the input module setting a match is not found in the specification as originally filed. Irrespective of whether or not there is any confusion of what the application actually discloses or what the appellant intended on

[1] See 37 CFR 41.50(a)(1) and MPEP 1211.

claiming (as evidenced by the attempt to amend the claim after the final rejection consistent with the examiner's interpretation set forth in the Final Rejection), the examiner is still required to reject the claims as written. As presented, the claim simply is not supported by specification as originally filled.

B. Rejection of claims 39-41 under 35 U.S.C. 102(e) as being anticipated by Dokic

Appellants argue that there is no indication in the cited portion of Dokic that the host processor [106] controls storage of desired packet identifiers and associated control information in the memory [205]. The claim is not limiting with respect to what is meant by 'associated control information'. Dokic teaches that the memory [205] stores both a PID filtering table (Col 8, Lines 20-52) and program service information (PSI) including a program association table (PAT) and a program map table (PMT) (Col 8, Lines 53-60). Subsequently, the claim is considered met in a number of ways.

In a first method, appellants argue that the PID filtering table does not contain associated control information or that responsive to a match the system retrieves from the memory control information associated with the desired packet identifier. The examiner respectfully disagrees. The PID filtering table contains 'control information' that not only identifies the PID itself, but also identifies the particular type of PID (audio, video, or data) and timing information (PCR) used to drive the decoding operations. For example, the creation of the PID filtering table by the host processor [106] in memory [205] effectively stores both the PID of interest as well as logical 'associated control information' that serves to identify the type of PID. This information is subsequently retrieved in conjunction with the matching

process (ex. What kind of PID did I match?) and is used to direct the processing as appropriate (Col 8, Lines 34-37 and 65-68). Alternatively, the processor [106] stores desired packet identifiers corresponding to the audio and video programs and associated control information corresponding to the clock references that driving the timing of the decoding of those desired packets. Subsequently, responsive to a match of a audio or video PID, the system controls the processing/decoding of those packets based upon the previously control information or derived program clock.

In a second method pertaining to the use of a 'default program', appellant argues that the there is no suggestion in Dokic that the host processor [106] controls the storage of default PIDs in the memory [205] (or the storage of associated control information in the memory [205]). Dokic teaches that the memory [205] stores program specific information (PSI) including a program association table (PAT) and a program map table (PMT) (Col 8, Lines 53-60). As understood in the art, the PMT identifies what PIDs correspond to different data types (audio, video, data) (Col 1, Line 60 – Col 2, Line 2; Col 2, Lines 28-44). This information serves as 'control information' because it is used by the receiver [100] to direct a particular PID to the appropriate decoder [120/122] (audio or video)(Col 8, Lines 65-68). Contrary to appellant's argument, the reference teaches that the host microprocessor ultimately 'controls' or directs the operations of the receiver [100] (Col 6, Lines 1-5; Col 13, Lines 63-65). Therefore, it is does not appear unreasonable to conclude that the host processor [106] also controls the particular storage of control information in the form of the PSI tables and subsequently utilizes this associated information to direct the packets to the

appropriate decoder. Accordingly, the examiner respectfully disagrees that the rejection of claims 39-41 under 35 U.S.C. 102(e) as being anticipated by Dokic is improper.

C. Rejection of claims 45 and 46 under 35 U.S.C. 102(e) as being anticipated by Dokic

As noted, appellants argue that Dokic does not teach, motivate, or suggest "receiving control information associated with a received data packet" as recited in claim 45. Consistent with the specification and its equivalents, the examiner has relied upon the digital signal processor [102] as the 'means retrieving control information" (equivalent to the transport processor [302] and SRAM [400]) and the host microprocessor [106] as the 'means for controlling processing' (equivalent to main processor - IA: Page 13, Lines 26-29). As previously noted, the claim does not specify what in particular 'control information' entails. The limitation could be met either by the stored information that defines the type of PID (audio, video, or data) for directing the PID to the appropriate decoder or information that is subsequently utilized to define the timing information (Dokic: Col 8, Lines 24-52). Accordingly, the examiner respectfully submits that Dokic anticipates claims 45 and 46.

D. Rejection of claims 11 and 13-20 under 35 U.S.C. 103(a) as being obvious over Dokic in view of the 'Manual'

Appellants argue that the Dokic is not an appropriate primary reference because the Examiner is using an unreasonable interpretation of the claimed memory since the examiner's interpretation of memory is not 'separate from the data stream'. In support, appellants argue that because the memory loads all data packets in the transport stream

whether the packets are required or not they are subsequently not 'separate from the data stream'. However, appellants later argue that the claims do not prohibit the memory from also storing data packets (or portions thereof). Based on appellant's remarks that the claims do not prohibit the memory from also storing data packets, the scope of 'separate from' would appear to be properly interpreted as still allowing for the storage of the transport or data stream.

Consistent with MPEP 2111 and its guidance on giving claims their broadest reasonable interpretation, the examiner has interpreted "separate from" simply to mean that both the data stream and the memory are distinctive or dissimilar entities in their own rights. For example, the memory [200/202/205] is a distinctive type or separate element regardless of its particular storage of data. As illustrated in Figure 5 of Dokic, the memory [200/202/205] is illustrated as being 'separate from' the MPEG-2 Transport stream. A similar interpretation of the meaning/scope of being 'separate from' likewise finds basis in the application given that the SRAM [400] and are distinctive or dissimilar entities as illustrated in Figures 1 and 2 as further noted in appellant's arguments. Accordingly, it is not believed that the examiner's interpretation of the Dokic memory being 'separate from the data stream' is unreasonable absent further amendment to limit the scope of being 'separate from'.

E. Rejection of claims 21-38 under 35 U.S.C. 103(a) as being obvious over Dokic in view of Blatter

Appellants argue that the examiner has not established a prima facie case of obvious on the basis that the examiner has failed to identify how to combine unit [45] of Blatter with

Dokic and that one having ordinary skill in the art would not have been motivated to combine the references since doing so would change the principles of operation of Dokic.

The DSP of Dokic comprises an analogous "memory structure" [205] to data SRAM [400] of the application since it stores packet information that enables the decoder to demultiplex and appropriately process the received transport stream by identifying packets of interest. The Blatter reference discloses a similar structure [45]. This is construed as meeting both the claimed "first data structure" and "second data structure" because it comprises both "addressing information that is accessed based on packet identifiers" and "control information that is accessed based on addressing information extracted from the first data structure" (Blatter: Col 4, Line 56 – Col 5, Line 18) in conjunction with the particular usage of memory mapping between control and/or encryption information and particular packet identifies which are retrieved in association with the processing of the received packets. This is similar to the usage of the logical "first" and "second data structures" utilized/described in instant application (IA: Page 10, Lines 3-21). Accordingly, the particularly proposed combination merely to utilizes known memory management techniques in a similar structure in order to improve Dokic by enabling it to support commonly utilized encryption/decryption using an efficient data management method (i.e. pointers as opposed to storing multiple copies of the same information in multiple locations).

Appellant argues that the proposed combination is also improper because the proposed modification would defeat the purpose of limiting the capabilities of the digital signal processor and therefore be contrary to 'speeding up the demultiplexing'. The proposed modification is in fact not fundamentally changing the operation of the Dokic as opposed to

modifying it using known techniques to improve a similar device. Dokic is directed towards MPEG signal demultiplexing using a decoupled architecture to process PSI information. It does not particularly teach away from all modifications to what may be considered as a necessary part of a limited interpretation process in order to generate a usable picture or other modifications associated with faster processing of PSI information. Rather, it is the usage of a decoupled architecture as opposed to the prior art method of having a non-decoupled architecture is what is 'speeding' Dokic up since the PSI tables are not being transferred between the demultiplexor and the microprocessor (Col 3, Line 35 – Col 4, Line 5). The proposed modification does not change the principle of operating with a decoupled architecture. It simply modifies the system to advantageously support the processing of encrypted programming. Accordingly, the particular modification to the existing memory structure of Dokic so as to further comprise additional structural information associated with the particular interpretation of a received transport stream should not be considered to be taught away from by the reference itself.

F. Rejection of claim 42 under 35 U.S.C. 103(a) as being obvious over Dokic in view of Bestler

Appellant's sole argument is that a prima facie case of obvious was not established because one was not established for the independent claim 39. As previously set forth, the rejection of claim 39 is believed proper. Therefore, absent any additional arguments, the rejection of claim 42 is believed proper.

G. Allowable subject Matter of claims 43-44

Appellant's sole argument is that claims 43-44 depend from an improperly rejected claim and subsequently the objection is improper. As previously set forth, the rejection is believed proper and the corresponding objection is proper given that the claims depend from a validly rejected base claim.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

SEB

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